## ABSTRACT

The invention describes a modification of FIFO hardware to allow improved use of FIFOs for burst reading from or writing to a processor direct memory access unit via either an expansion bus or an external memory interface using FIFO flag initiated bursts. The hardware and FIFO signal modifications make the FIFO-DMA interface immune to deadlock conditions and generation of spurious interrupt events in the process of initiating burst transfers. The FIFO function is modified to synchronize the frame transfer on the digital signal processor even if the digital signal processor lacks this functionality. By delaying the programmable flag assertions within the FIFO until after the current burst is complete the DSP-FIFO interface may be made immune to deadlock conditions and generation of spurious events.